Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **1A**
2. **N. 1Y**
3. **2A**
4. **N. 2Y**
5. **3A**
6. **N. 3Y**
7. **GND (2 pads)**
8. **N. 4Y**
9. **4A**
10. **N. 5Y**
11. **5A**
12. **N. 6Y**
13. **6A**
14. **VCC (2 pads)**

**.051”**

**.056”**

**1 14 14 13**

**7 7 8**

**MASK**

**REF**

**1**

**1**

**10**

**9**

**2**

**3**

**4**

**9**

**6**

**J004X**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: VCC**

**Mask Ref: J004X**

**APPROVED BY: DK DIE SIZE .051” X .056” DATE: 5/9/19**

**MFG: FAIRCHILD THICKNESS .014” P/N: 54ACT04**

**DG 10.1.2**

#### Rev B, 7/19/02